Q.P. Code: 16EC424 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech III Year II Semester Supplementary Examinations Dec 2019

DIGITAL IC APPLICATIONS

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Draw the circuit diagram of basic CMOS gate and explain the operation.	**6M**
	b	Compare CMOS, TTL and ECL logic families.	**6M**

OR

2	**a**	What is the difference between transition time and propagation delay? Explain these two parameters with reference to CMOS logic.	**6M**
	b	Explain sinking current and sourcing current of TTL Output. Which of the above parameters decide the fan out and how?	**6M**

UNIT-II

3		Draw and explain in detail of VHDL design flow.	**12M**

OR

4	**a**	Design the logic circuit and write VHDL program for the following functions. $F(X) = \sum A, B, C, D (0, 2, 5, 7, 8, 10, 13, 15) + d (1, 6, 11)$.	**6M**
	b	Design the logic circuit and write VHDL program for the following functions. $F(Y) = \prod A, B, C, D (1, 4, 5, 7, 9, 11, 12, 13, 15)$.	**6M**

UNIT-III

5	**a**	With the help of logic diagram explain 74×157 multiplexer.	**6M**
	b	Write the data flow style VHDL program for this IC.	**6M**

OR

6	**a**	Draw the logic symbol of 74 x 85, 4-bit comparator and write a VHDL code for it.	**6M**
	b	Design a 16-bit comparator using 74×85 ICs.	**6M**

UNIT-IV

7		Design an 8 bit parallel in and serial out shift register. Explain the operation of the above Shift register with the help of timing waveforms.	**12M**

OR

8	**a**	Distinguish between the synchronous and asynchronous counters.	**6M**
	b	What are the impediments to synchronous design?	**6M**

UNIT-V

9		Design a barrel shifter for 8-bit using three control inputs. Write a VHDL program for the same in data flow modeling.	**12M**

OR

10	**a**	Distinguish between latch and flip flop. Show the logic diagram for both. Explain the operation with the help of function table.	**6M**
	b	Write a VHDL code for a D-flip flop in behavioral model.	**6M**

*** END ***